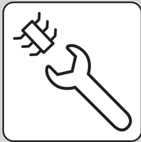
PROJECT RESULT



Technology platform for next-generation core CMOS process

2A702: Manufacturing test technologies for SoC and SIP (NanoTEST)

Advanced test technologies cut costs and time to market for advanced chip manufacture

Chip testing has become an increasingly significant part of total production costs in recent years, as manufacturing techniques have advanced into the nanotechnology arena and automated production has shortened time-to-market. Advanced test technologies are required to detect defects becoming apparent at such levels, particularly for system-on-chip (SoC) and system-in-package (SIP) applications. The NanoTEST project has developed advanced and innovative test methods that reduce costs and slash the time required – speeding the introduction of new products in the latest technologies in Europe.

Testing has taken on an increasingly important role in the manufacturing process for system-on-chip (SoC) and system-in-package (SIP) semiconductor production in recent years. The main reasons are the growing device complexity made possible by new wafer fabrication techniques, a higher cost-of-ownership for test equipment and longer test-execution times per chip.

Such pressures are combined with ever-increasing demands for higher product quality, shorter time to market and lower costs. The result is a view that the test process needs radical upgrading if it is to keep pace with the needs of chip manufacturing in the nanotechnology era. With semiconductor manufacturing now advancing into the 65 nm and 45 nm nodes, the MEDEA+ 2A702 NanoTEST project set out to develop more advanced test methodologies for SoC and SIP testing, together with the associated test flows, tools and standards.

The NanoTEST consortium brought together four European chipmakers, three well-known research institutes and two small and medium-sized enterprises (SMEs).

Developing new test methods

Project tasks were split into three main areas: the first investigated what defects occur in new manufacturing processes, and focused on developing new methods to measure those defects, particularly in mixed analogue-digital circuits; the second area addressed what was needed at the design stage in order to make the new test approaches possible; and the third concentrated on applying the approaches developed in the first two areas to decrease the overall cost of testing and automate the creation of new test programs.

By the end of the project, NanoTEST consortium partners managed to reduce costs per test process – a key objective – by:

- A factor of up to 20 in digital testing;
- Over ten times in memory testing;
- Up to four times in analogue and mixed-signal (AMS) testing – parallel concurrent testing enabled by design for testability (DfT) and built-in self-test (BIST); and
- Up to four times in radio frequency (RF) testing.

NanoTEST also obtained a 50% reduction in time-to-market due to shorter test times, while zero-defect programmes have been developed for improved quality. The quality results however depend on application area. Automotive sector applications put an enormous focus on quality – down to zero parts per million (ppm) – while quality levels for mobile phone applications are much lower.

Numerous conference papers

Not only did NanoTEST partners achieve all

the goals they set out to reach, they have also submitted over 300 papers on manufacturing test technologies at key scientific conferences such as DATE, ITC, VTS and ETS. Many of these presentations were combined publications and papers from respected industry and research institutes, and a number of 'best paper' awards were received during the project.

NanoTEST partners have also been active on programme committees, steering committees and as topic chairs in all major conferences and workshops on manufacturing test processes. They have submitted new approaches to test methodologies for SoC and SIP manufacturing, and have been heavily involved in standardisation activities such as IEEE1149.4 AMS Test Bus, IEEE P1149.7 Debug and Test Interface, AEC-Q100 automotive IC stress, and IEEE 1450 standard test interface for AMS (STIL_AMS).

The ideas and approaches developed during NanoTEST have also been disseminated as part of the research process. Over the four-year term of the project, some 24 MSc students and 36 PhD students from participating academic institutes have been involved.

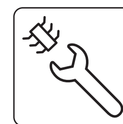
Efficient automatic testing

Many of the consortium partners have already applied the technologies and approaches developed within the NanoTEST project to their own product development and manufacturing cycle. One of the chipmakers, for example, is active in the automotive, medical and aerospace markets, where quality and reliability are key concerns. In these markets, customers tend to expect failure rates of equal to or less than one ppm defects delivered.

Functional testing alone to ensure a design meets specifications cannot meet the cost-reduction and time-to-market parameters required for market success at nanotechnology levels. The partners therefore developed an automatically generated test programme that was able to construct a high-level AC amplifier test. The input file for the circuit was populated with the relevant parameters, then the high-level module run successfully. Once completed, a test module using actual test instruments was generated, still utilising a tester-independent language.

The consortium partners found that they were able to generate a mixed-signal test program shell – about 30% of the complete program – in about a day, and debug it in one engineering tester session of about four hours. They achieved a test-development cost-reduction of about 25%, and reduced the debugging effort – time on the tester – by around 20%. As a result, these tools and methods are now being adopted as mainstream test development tools.

Semiconductor manufacturers involved in this project – Infineon, NXP, On Semiconductors and STMicroelectronics – are all highly active in the consumer, automotive and telecommunications markets. The advances achieved within NanoTEST will enable them to continue growth in SoC applications, as well as apply SIP, within a much more cost-competitive environment. The test technologies developed under NanoTEST will be key contributors to the commercial success of products in the new technology nodes, and thus to the competitiveness of the European microelectronics industry.



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PARTNERS:

CEA-LETI
Infineon
LIRMM
NXP Semiconductors
On Semiconductors (formerly AMIS)
Philips
Q-Star Test
Temento
STMicroelectronics
TIMA

PROJECT LEADER:

Kees Veelenturf
NXP Semiconductors

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COUNTRIES INVOLVED:

Austria
Belgium
France
The Netherlands

MEDEA+ Office
140bis, Rue de Rennes
F-75006 Paris
France
Tel.: +33 1 40 64 45 60
Fax: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

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MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.